IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) A semiconductor device comprising:

a first main electrode;

a second main electrode;

a semiconductor base region of a first conductivity type;

a gate electrode provided in a trench through an insulating film, the trench being formed to penetrate the semiconductor base region; and

a first semiconductor region of a ~~first~~ second conductivity type provided under the semiconductor base region and a second semiconductor region of a ~~second~~ first conductivity type provided under the first semiconductor ~~base~~ region,

a flow of a current between the first and second main electrodes when a voltage of a predetermined direction is applied between these electrodes being controllable in accordance with a voltage applied to the gate electrode, and

a depleted region extending from a junction between the first and the second semiconductor regions reaching the trench.

2. (Original) The semiconductor device according to claim 1, wherein a forward voltage is applied to a p-n junction formed between the first and second semiconductor regions when the voltage of the predetermined direction is applied between the first and second main electrodes.

3. (Currently Amended) The semiconductor device according to claim 1, wherein the ~~first~~ second semiconductor region is in contact with the trench.

4. (Currently Amended) The semiconductor device according to claim 1, wherein a bottom of the trench is provided within the ~~first~~ second semiconductor region.

5. (Original) The semiconductor device according to claim 1, wherein a plurality of the first semiconductor regions and a plurality of the second semiconductor regions are laminated alternately under the semiconductor base region.

6. (Currently Amended) The semiconductor device according to claim 1, wherein the ~~first~~ second semiconductor region is provided apart from the trench.

7. (Currently Amended) The semiconductor device according to claim 1, wherein a plurality of the first semiconductor ~~regions~~ region and ~~a plurality of~~ the second semiconductor ~~regions~~ region are arranged alternately on a plane which is substantially perpendicular to a depth direction of the trench.

8. (Original) A semiconductor device comprising:

a first semiconductor region of a second conductivity type;

a second semiconductor region of a first conductivity type provided on the first semiconductor region,

a third semiconductor region of a second conductivity type provided on the second semiconductor region,

a fourth semiconductor region of a first conductivity type provided on the third semiconductor region,

a fifth semiconductor region of a second conductivity type provided on the fourth semiconductor region,

a trench penetrating at least the third through fifth semiconductor regions, a bottom of the trench being provided within the second semiconductor region; and

a gate electrode provided in the trench through an insulating film.

9. (Original) The semiconductor device according to claim 8, wherein the second and the third semiconductor regions are substantially depleted.

10. (Original) The semiconductor device according to claim 8, wherein a carrier concentrations of the second and the third semiconductor regions are equal to or less than 3×10^{16} /cm^3.

11. (Original) The semiconductor device according to claim 8, wherein a carrier concentrations of the second and the third semiconductor regions are equal to or less than 5×10^{15} /cm^3.

12. (Original) A semiconductor device comprising:

a first semiconductor region of a second conductivity type;

a second semiconductor region of a first conductivity type provided on the first semiconductor region,

a third semiconductor region of a second conductivity type provided on the second semiconductor region,

a fourth semiconductor region of a first conductivity type provided on the third semiconductor region,

a fifth semiconductor region of a second conductivity type provided on the fourth semiconductor region,

a trench penetrating at least the third through fifth semiconductor regions, a bottom of the trench being provided between an upper surface and a lower surface of the second semiconductor region;

a sixth semiconductor region of a second conductivity type provided in contact with the bottom of the trench; and

a gate electrode provided in the trench through an insulating film.

13. (Original) The semiconductor device according to claim 12, wherein the sixth semiconductor region is substantially depleted by a junction with the second semiconductor region.

14. (Original) The semiconductor device according to claim 12, wherein the second and the third semiconductor regions are substantially depleted.

15. (Original) The semiconductor device according to claim 12, wherein a carrier concentrations of the second and the third semiconductor regions are equal to or less than 3×10^{16} /cm^3.

16-19. (Canceled)

20. (Currently Amended) ~~The semiconductor device according to claim 16,~~ A semiconductor device comprising:

a first semiconductor region of a second conductivity type;

a semiconductor layer provided on the first semiconductor region and having a plurality of second semiconductor regions of a first conductivity type and a plurality of third semiconductor regions of a second conductivity type, the second and the third semiconductor regions being arranged alternately;

a fourth semiconductor region of a first conductivity type provided on the semiconductor layer,

a fifth semiconductor region of a second conductivity type provided on the fourth semiconductor region,

a trench penetrating at least the fourth and the fifth semiconductor regions, a bottom of the trench being provided within the semiconductor layer; and

a gate electrode provided in the trench through an insulating film,

wherein carrier concentrations of the second and the third semiconductor regions are equal to or less than 5×10^{15} /cm^3.

21. (New) The semiconductor device according to claim 1, wherein the second semiconductor region is in contact with a side of the trench, but is not in contact with a bottom of the trench, and a semiconductor region of a first conductivity type is provided instead.

22. (New) A semiconductor device comprising:

a first semiconductor region of a second conductivity type;

a semiconductor layer provided on the first semiconductor region and having a plurality of second semiconductor regions of a first conductivity type and a plurality of third semiconductor regions of a second conductivity type, the second and the third semiconductor regions being arranged alternately along with two diagonal directions on the first semiconductor region;

a fourth semiconductor region of a second conductivity type provide don the fourth semiconductor region,

a fifth semiconductor region of a second conductivity type provided on the fourth semiconductor region,

a trench penetrating at least the fourth and the fifth semiconductor regions, a bottom of the trench being provided within the semiconductor layer; and

a gate electrode provided in the trench through an insulating film.

23. (New) The semiconductor device according to claim 22, wherein the second and the third semiconductor regions are substantially depleted.

24. (New) The semiconductor device according to claim 20, wherein a carrier concentrations of the second and the third semiconductor regions are equal to or less than $3 \times 10^{17}/cm^3$.

25. (New) The semiconductor device according to claim 20, wherein a carrier concentrations of the second and the third semiconductor regions are equal to or less than $3 \times 10^{16}/cm^3$.